## REMARKS

Claims 1-12 are pending in the application.

Claims 1-12 have been rejected.

I. REJECTION UNDER 35 U.S.C. § 102

Claims 1-12 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Publication No. 2003/0224747 to *Anand* (hereinafter "Anand"). The rejection is respectfully traversed.

A cited prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single cited prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

**CLAIM 1**

Independent Claim 1 recites a pulse detection unit, for detecting pulses in a received signal. The pulse detection unit includes a plurality of comparators; a sampling time generator, for generating signals indicative of a plurality of sampling time points; and a reference level generator, for generating a plurality of reference levels. The claim further recites that each of the comparators is programmable with a sampling time point selected from said plurality of sampling time points and with a reference level selected from said plurality of reference levels, and that the received signal is applied to each of the comparators such that each of the comparators produces a respective output signal based on a comparison between the received signal level and the selected reference level at the selected sampling time point.

Applicants submit that *Anand* does not disclose each and every limitation found in independent Claim 1. In particular, the Applicants submit that *Anand* does not disclose a sampling time generator, for generating signals indicative of a plurality of sampling time points. The Office

Action argues that *Anand* (paragraph [0058]) teaches a sampling time generator for generating signals indicative of a plurality of sampling points. The Office Action states "the charge pump feedback bias signal may be sampled."

*Anand* describes a phase-locked loop circuit including an array of selectable capacitors formed within the phase-locked loop circuit to enable the phase-locked loop circuit to provide a degree of course frequency control by adding or removing capacitors and a degree of fine frequency control by sinking or sourcing current from a charge pump into a loop filter. Further, *Anand* teaches that a finite state machine is provided within a voltage controlled oscillator calibration circuit that communicates with an external base-band processor to initiate a calibration process, and further to determine how many capacitors of an array of capacitors is formed within the phase-locked loop circuit should be coupled to provide the course frequency control (*Anand*, Abstract).

*Anand*, however, fails to disclose "a sampling time generator, for generating signals indicative of a plurality of sampling time points; ....., wherein each of the comparators is programmable with a sampling time point selected from said plurality of sampling time points ....., and wherein the received signal is applied to each of the comparators such that each of the comparators produces a respective output signal based on the comparison between the received signal level and the selected reference level at the selected sampling time point". In particular, *Anand* does not teach a sampling time generator or any selected sampling time points because the voltage control oscillator (VCO) produces a signal having a frequency characteristic that is a function of an input voltage level of the VCO. (*Anand*, paragraph [0009]).

In addition, the Office Action cites the *Anand*'s charge pump feedback bias (CPFB) signal to teach the generating signal(s) indicative of a plurality of sampling points. (Office Action, page 2). However, the Office Action also cites *Anand*'s charge pump feedback bias (CPFB) signal as the received signal. (Office Action, page 3). *Anand* does not disclose or teach that the CPFB signal is both the "generated signals indicative of a plurality of sampling points" and "a received signal applied to each of the comparators," as recited in Applicants' claims. Further, *Anand* does not describe "the received signal" as recited in independent Claim 1.

*Anand* provides a circuit that reduces the required gain level for the VCO and therefore reduces any introduced phase noise while accurately producing a signal with a specified frequency. (*Anand*, paragraph [0010]). *Anand* (paragraph [0058]) cited by the Office Action merely describes the calibration circuit of the VCO. Morever, the logic circuitry comprised by the finite state machine operates in the frequency domain. Thus the charge pump feedback bias signal cannot be interpreted as signals indicative of a plurality of sampling time points generated by a sampling time generator.

Accordingly, the Applicant respectfully requests the Examiner withdraw the § 102(b) rejection of Claim 1 and its dependent claims.

**CLAIM 7**

The Office Action asserts that the limitations of Claims 7-12 are similar to those found in Claims 1-6 and rejects Claims 7-12 based on the same rationale. Therefore, these claims are allowable for at least the same, or similar, reasons as Claims 1-6, discussed above. Accordingly, the Applicants respectfully request withdrawal of the § 102(b) rejection of Claims 7-12.

## II. CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***rmccutcheon@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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